CLAIMS:

1. A Snoop Filter for use in a multi-node processor system including different nodes of multiple processors and corresponding processor caches, comprising:

a cache array to store data information in a plurality of lines; and

a replacement mechanism responsive to a processor transaction to identify a least-recently-used (LRU) line from the plurality of lines in the cache array for update to reflect lines that are replaced in one or more processor caches.

2. The Snoop Filter as claimed in claim 1, wherein the processor transaction indicates one of a processor memory read – as a result of a processor cache MISS (RM), a processor read for ownership (RO), a clean line replacement (CLR), and a processor write (W).

3. The Snoop Filter as claimed in claim 1, wherein the cache array is a set-associative cache.

4. The Snoop Filter as claimed in claim 1, wherein the cache array comprises:

a plurality of sets where each set is made up of a number of lines in the Snoop Filter; and

a least-recently-used (PLRU) vector field to select which line or way to replace.

5. The Snoop Filter as claimed in claim 4, wherein each set in the cache array has a vector of "n" bits depending on the associativity of the cache which can be decoded to identify the PLRU way within the set.

6. The Snoop Filter as claimed in claim 5, wherein each processor transaction includes an address where a portion of the address is used to identify the set (set index), and another portion of the address is used to uniquely identify the line in the Snoop Filter.

7. The Snoop Filter as claimed in claim 6, wherein the Pseudo Least-Recently-Used (PLRU) replacement mechanism is configured to determine if there is a HIT or a MISS in response to receipt of the processor transaction, and when there is a HIT, set an entry (way) as a most-recently used (MRU) and update selected LRU bits to their complement, or when there is a MISS, set an entry (way) to MRU.

8. The Snoop Filter as claimed in claim 1, wherein the PLRU replacement mechanism is configured to:

determine if the processor transaction is one of a processor memory read (RM) and a processor read for ownership (RO);

if the processor transaction is one of a processor memory read (RM) and a processor read for ownership (RO), determine if the cache array has a line associated with the processor transaction;

if the cache array has a line associated with the processor transaction indicating a HIT condition, select a corresponding entry (way) as a most-recently used (MRU); and

if the cache array does not have a line associated with the processor transaction indicating a MISS condition, select a victim entry (way) using a LRU vector and make the victim entry (way) as MRU.

9. The Snoop Filter as claimed in claim 8, wherein the PLRU replacement mechanism is further configured to:

determine if the processor transaction is one of a clean line replacement (CLR) and a processor write (W); and

if the processor transaction is one of a clean line replacement (CLR) and a processor write (W), select a corresponding way as LRU.

10. A Pseudo Least-Recently-Used (PLRU) replacement method for a multi-node Snoop Filter including a plurality of lines storing data information, comprising:

determining if a processor transaction is one of a processor memory read (RM), a processor read for ownership (RO), a clean line replacement (CLR), and a processor write (W);

determining if a Snoop Filter cache array has a line associated with the processor transaction, if the processor transaction is one of the processor memory read (RM) and the processor read for ownership (RO);

if the cache array has a line associated with the processor transaction indicating a HIT condition, selecting a corresponding entry (way) as a most-recently used (MRU);

if the cache array does not have a line associated with the processor transaction indicating a MISS condition, selecting a victim entry (way) using a LRU vector and making the victim entry (way) as MRU; and

selecting a corresponding way as LRU, if the processor transaction is one of the clean line replacement (CLR) and the processor write (W).

11. The Pseudo Least-Recently-Used (PLRU) replacement method as claimed in claim 10, wherein the Snoop Filter is organized as a set-associative cache.

12. The Pseudo Least-Recently-Used (PLRU) replacement method as claimed in claim 11, wherein the Snoop Filter cache comprises:

a plurality of sets where each set is made up of a number of lines in the Snoop Filter; and

a least-recently-used (PLRU) vector field to select which line or way to replace.

13. The Pseudo Least-Recently-Used (PLRU) replacement method as claimed in claim 12, wherein each set in the cache array has a vector of "n" bits depending on the associativity of the cache which can be decoded to identify the PLRU way within the set.

14. A multi-node processor system, comprising:

one or more processor nodes each including a plurality of processors with processor caches ;

one or more I/O nodes each including an I/O bridge with a private I/O cache; and

a Snoop Filter operatively connected to the processor nodes and the I/O nodes to manage data information related to cache lines in one or more processor caches, said Snoop Filter comprising a cache array to store data information in a plurality of lines, and a Pseudo Least-Recently-Used (PLRU) replacement mechanism responsive to a processor transaction to identify a least-recently-used (LRU) line from the plurality of lines in the cache array for update to reflect lines that are replaced in one or more processor caches.

15. The multi-node processor system as claimed in claim 13, wherein the processor transaction indicates one of a processor memory read – as a result of a processor cache MISS (RM), a processor read for ownership (RO), a clean line replacement (CLR), and a processor write (W).

16. The multi-node processor system as claimed in claim 14, wherein the cache array is a set-associative cache.

17. The multi-node processor system as claimed in claim 14, wherein the cache array comprises:

a plurality of sets where each set is made up of a number of lines in the Snoop Filter; and

a least-recently-used (PLRU) vector field to select which line or way to replace.

18. The multi-node processor system as claimed in claim 17, wherein each set in the cache array has a vector of "n" bits depending on the associativity of the cache which can be decoded to identify the PLRU way within the set.

19. The multi-node processor system as claimed in claim 18, wherein each processor transaction contains an entry address of an entry (way) in the cache array including a memory location tag used to identify a unique cache entry, and a set index used to identify the set of entries.

20. The multi-node processor system as claimed in claim 14, wherein the Pseudo Least-Recently-Used (PLRU) replacement mechanism is configured to determine if there is a HIT or a MISS in response to receipt of the processor transaction, and when there is a HIT, set an

entry (way) as a most-recently used (MRU) and update selected LRU bits to their complement, or when there is a MISS, set an entry (way) to MRU.

21. The multi-node processor system as claimed in claim 14, wherein the PLRU replacement mechanism is configured to:

determine if the processor transaction is one of a processor memory read (RM) and a processor read for ownership (RO);

if the processor transaction is one of a processor memory read (RM) and a processor read for ownership (RO), determine if the cache array has a line associated with the processor transaction;

if the cache array has a line associated with the processor transaction indicating a HIT condition, select a corresponding entry (way) as a most-recently used (MRU); and

if the cache array does not have a line associated with the processor transaction indicating a MISS condition, select a victim entry (way) using a LRU vector and make the victim entry (way) as MRU.

22. The multi-node processor system as claimed in claim 21, wherein the PLRU replacement mechanism is further configured to:

determine if the processor transaction is one of a clean line replacement (CLR) and a processor write (W); and

if the processor transaction is one of a clean line replacement (CLR) and a processor write (W), select a corresponding way as LRU.